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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,152	10/21/2003	Gregory Starr	ALT-256	6613

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,152	STARR, GREGORY	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003 and 05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,32-48 and 77-84* is/are rejected.

7)☒ Claim(s) *4-31 and 49-76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-84 are presented in the instant application according to the Applicant' filing on 10/21/2003.

Drawings

1. The drawings are objected to because of the following informality:

Fig. 1, box 17, "-M" should be changed to -- ÷M-- .

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 32-33, 35-48, 77-78, and 80-84 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (U.S. Patent No. 6,448,820).

With respect to claims 1 and 46, Wang et al. discloses, in Figs. 1,2 4A-B and 5, a phase-locked loop circuit [Fig. 5] for use in a programmable logic device, the phase-locked loop circuit having an input terminal for receiving an input signal [Fig. 5, REF] having a reference frequency and an output terminal for outputting an output frequency [Fig. 5, 510] phase-locked to the reference frequency, and comprising an oscillator [Fig. 5, 533] for producing the output frequency; and a feedback path feeding the oscillator, the feedback path accepting as inputs the reference frequency and the output frequency, and causing the oscillator to drive the output frequency to a phase-frequency lock with the reference frequency, the feedback path comprising

at least one component connected therein; wherein at least one of at least one component is also connected to another portion of programmable logic device [Fig. 1, 121] for operation of the another portion of the programmable logic device with the at least one of the at least one component.

With respect to claims 2 and 47, Wang et al. discloses, in Figs. 1, 2 4A-B and 5, that when the phase-locked loop circuit is not in use in the programmable logic device, the at least one of

the at least one component is available for use by the another portion of the programmable logic device.

With respect to claims 3 and 48, Wang et al. discloses, in Figs. 1, 2 4A-B and 5, that when the phase-locked loop circuit is in use in the programmable logic device, the another portion of

the programmable logic device is available to be substituted in the phase-locked loop circuit for the at least one of the at least one component.

With respect to claims 32 and 77, Wang et al. discloses, in Fig. 5, that the oscillator is a voltage-controlled oscillator.

With respect to claims 33 and 78, Wang et al. discloses, in Fig. 5, an output scaling counter [539] downstream of said output terminal.

With respect to claims 35 and 80, Wang et al. discloses, in Fig. 5, a feedback scaling counter [539] between output terminal and feedback path.

With respect to claim 36, Wang et al. discloses, in column 5, lines 61-62, that a programmable logic device comprising the phase-locked loop circuit.

With respect to claims 37 and 81, Wang et al. discloses, in Fig. 1, a digital processing system comprising a) processing circuitry [101]; b) a memory [105] coupled to the processing circuitry; and c) a programmable logic device [121] coupled to the processing circuitry and the memory.

With respect to claims 38 and 82, Wang et al. discloses, in Fig. 1 and column 3, lines 16-19, a printed circuit board on which is mounted a programmable logic.

With respect to claims 39 and 83, Wang et al. discloses, in Fig. 1 and column 3, lines 16-21, that the printed circuit board further comprising memory circuitry [105] mounted on the printed circuit board and coupled to the programmable logic device [121].

With respect to claims 40 and 84, Wang et al. discloses, in Fig. 1 and column 3, lines 16-21, that the printed circuit board further comprising processing circuitry [101] mounted on the printed circuit board and coupled to the memory circuitry [105].

With respect to claim 41, Wang et al. discloses, in Fig. 1 and column 3, lines 16-21, an integrated circuit device comprising the phase-locked loop circuit.

With respect to claim 42, Wang et al. discloses, in Fig. 1 and column 3, lines 16-21, a digital processing system comprising processing circuitry; a memory coupled to said processing circuitry; and an integrated circuit device coupled to the processing circuitry and the memory.

With respect to claim 43, Wang et al. discloses, in Fig. 1 and column 3, lines 16-21, a printed circuit board on which is mounted an integrated circuit device.

With respect to claims 44, Wang et al. discloses, in Fig. 1 and column 3, lines 16-21, that the printed circuit board further comprising memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

With respect to claim 45, Wang et al. discloses, in Fig. 1 and column 3, lines 16-19, that the printed circuit board further comprising processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 34 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,448,820) in view of Linebarger et al. (U.S. Patent No. 6, 141, 394).

With respect to claims 34 and 79, Wang et al. discloses all of the claimed limitations as expressly recited in claims 1 and 46, except for the phase locked loop comprising an input scaling counter upstream of the input terminal.

Linebarger et al. discloses, in Fig. 4, a scaling counter [111] being coupled to the input of the phase detector [106] of a phase locked loop.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a scaling counter connected to the input terminal to enable comparing frequencies that have similar values since such circuit arrangement of the scaling counter would enhance the synchronization process of the phase locked loop.

Allowable Subject Matter

6. Claims 4-31 and 49-76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

• A phase-locked loop circuit, in which an at least one component comprises an analog front end circuit having the comparison signal as an input and outputting an analog voltage signal indicative of a comparison; an analog-to-digital converter having the analog voltage signal as an input and outputting a digitized voltage signal; a digital signal processor having the digitized voltage signal as an input and outputting a digital control signal; and a digital-to-analog converter having the digital control signal and outputting an analog control signal that is input to an oscillator, as called for in claims 4 and 49;

• A phase-locked loop circuit, in which an at least one component comprises a digital counter circuit having digital comparison signals as inputs and outputting digital count signals indicative of a comparison; a digital signal processor having the digital count signals as inputs and outputting a digital control signal; and a digital-to-analog converter having the digital control signal and outputting an analog control signal that is input to an oscillator, as called for in claims 21 and 66;

Citation of Relevant Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Moore (U.S. Patent No. 6,690,224) discloses architecture of a phase locked loop with dynamic frequency control on a programmable logic device.

Prior art Plants et al. (U.S. Patent No. 6,718,477) discloses a delay locked loop for an FPGA architecture.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER